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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/716,533 | 11/20/2003 | Hirotaka Tamura | 100021-00135 | 6886 |
| 4372 | 7590 | 10/22/2004 | EXAMINER | |
| ARENT FOX KINTNER PLOTKIN & KAHN 1050 CONNECTICUT AVENUE, N.W. SUITE 400 WASHINGTON, DC 20036 | | | LAM, TUAN THIEU | |
| | | ART UNIT | PAPER NUMBER | |
| | | | 2816 | |

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/716,533 | TAMURA ET AL. |
| | Examiner | Art Unit |
| | Tuan T. Lam | 2816 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 20 November 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-12, 16 and 17 is/are rejected.

7) Claim(s) 13-15 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 20 November 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a))

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/20/2003.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____ .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5-7 and 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 5 and 10, the recitation of “a first and a second resistor elements coupling the differential input signals” is indefinite because it is misdescriptive. Figure 3 shows the first and second resistors (131, 132) coupling to the differential output signals not the differential input signals. Correction is required.

Claims 6-7, 11-12 are indefinite because of the technical deficiencies of claims 5 and 10.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara et al. (USP 6,107,882). Figure 8A shows a buffer circuit (710) receiving differential input signals (Vin, Vin), output signals (Vout, Vout-), a common mode level generator circuit (not shown) for generating a specific level of a common mode voltage (Vref) for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (R1, R2, C1), a bias voltage

adjusting circuit (810) for adjusting a bias voltage to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit as called for in claims 1, 3.

Regarding claim 2, the output signals V_{out} , V_{out-} has a preferred common mode voltage V_{ref} is applied to a next stage circuit (not shown).

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto (USP 6,665,655). Figure 7 shows a buffer circuit (dashed box) receiving differential input signals (V_{in} , V_{in-}), output signals (V_{out} , V_{out-}), a common mode level generator circuit (not shown) for generating a specific level of a common mode voltage (V_{ref}) for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (resistors connected to V_{out+} and V_{out-}), a bias voltage adjusting circuit (comparator) for adjusting a bias voltage to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit as called for in claim 1.

Regarding claims 8-9, the common mode voltage detection circuit (resistors connected to V_{out+} , V_{out-}) detects a common mode voltage of output signals of said next stage circuit (circuit with a triangular symbols).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara et al. (USP 6,107,882) in view of Tichauer (USP 6,784,744). Figure 8A shows a buffer circuit (710) receiving differential input signals (V_{in} , V_{in}), output signals (V_{out} , V_{out-}), a common mode level generator circuit (not shown) for generating a specific level of a common mode voltage (V_{ref}) for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (R_1 , R_2 , C_1), a bias voltage adjusting circuit (810) for adjusting a bias voltage to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit. The Gabara et al. reference does not show a low pass filter (resistor 133 and capacitor 134 of figure 3 of the present invention) for processing the output of the common mode level generator (12) as called for in claim 4. Figure 1 of Tichauer shows a low pass filter (R_1 , C_1) for filtering a reference voltage (V_b) providing a noise free reference signal. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include the low pass filter in the circuit arrangement of Gabara et al. for the purpose of removing noise from the reference voltage V_{ref} and to provide accurate comparison reference voltage.

Regarding claim 5, the combination reference of Gabara et al. and Tichauer shows first, second and third resistors (R_1 , R_2 from Gabara et al., R_1 from Tichauer).

Regarding claim 6, the combination reference of Gabara et al. and Tichauer shows first and second capacitors (C1 of Gabara et al., and C1 of Tichauer).

Regarding claim 7, the comparator is seen as the comparator 810.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara et al. (USP 6,107,882) in view Jin et al. (USP 5,146,152). Figure 8A shows a buffer circuit (710) receiving differential input signals (Vin, Vin), output signals (Vout, Vout-), a common mode level generator circuit (not shown) for generating a specific level of a common mode voltage (Vref) for the output signals to be output from said buffer circuit, a common mode voltage detection circuit (R1, R2, C1), a bias voltage adjusting circuit (810) for adjusting a bias voltage to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit. The Gabara et al. reference does not show the common mode level generator circuit comprises a constant current source. Jin et al.'s figure 6 shows a reference voltage generator (common mode level generator circuit) generates a reference voltage independent of temperature variation comprising a current source 31. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to use Jin et al.'s reference voltage generator for generating the reference voltage because the Jin et al.'s reference voltage is independent of temperature variation.

Regarding claim 17, the Gabara et al. does not shows a voltage divider for generating the reference voltage. Figure 1 of Jin et al. shows a voltage divider (50) generating a reference voltage. Therefore, it would have been obvious to a person skilled in the art at the time of the

invention was made to use Jin et al.'s voltage divider for generating the reference voltage because it is simple to make and does not occupy lots of space on the chip.

Allowable Subject Matter

7. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. Claims 10-12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam
Primary Examiner
Art Unit 2816

10/19/2004